--- Current "arbiter" VHDL Code

--- Current file name: arbiter.vhd

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LIBRARY IEEE ;

USE IEEE.STD\_LOGIC\_1164.ALL ;

USE IEEE.STD\_LOGIC\_ARITH.ALL ;

ENTITY arbiter IS

PORT (clk : IN STD\_LOGIC ;

request0 : IN STD\_LOGIC ;

request1 : IN STD\_LOGIC ;

reset\_l : IN STD\_LOGIC ;

grant0 : OUT STD\_LOGIC ;

grant1 : OUT STD\_LOGIC) ;

END arbiter ;

ARCHITECTURE behavioral of arbiter IS

TYPE states IS (s0, s1, s2, s3) ;

SIGNAL state : states ;

SIGNAL nxt\_state : states ;

BEGIN

clkd:PROCESS(clk)

BEGIN

IF (clk'EVENT AND clk='1') THEN

IF (reset\_l = '0') THEN

state <= s0;

ELSE

state <= nxt\_state;

END IF;

END IF;

END PROCESS clkd;

state\_trans:PROCESS(request0,request1,state)

BEGIN

CASE state IS

WHEN s0 => IF (request0 = '1') THEN

nxt\_state <= s1 ;

ELSIF (request1 = '1') THEN

nxt\_state <= s2 ;

ELSE

nxt\_state <= s0 ;

END IF ;

WHEN s1 => IF (request0 = '1') THEN

nxt\_state <= s1 ;

ELSE

nxt\_state <= s3 ;

END IF;

WHEN s2 => IF (request1 = '1') THEN

nxt\_state <= s2 ;

ELSE

nxt\_state <= s0 ;

END IF;

WHEN s3 => IF (request1 = '1') THEN

nxt\_state <= s2 ;

ELSIF (request0 = '1') THEN

nxt\_state <= s1 ;

ELSE

nxt\_state <= s3 ;

END IF ;

END CASE ;

END PROCESS state\_trans ;

output:PROCESS(state)

BEGIN

CASE state IS

WHEN s0 =>

grant0 <= '0' ;

grant1 <= '0' ;

WHEN s1 =>

grant0 <= '1' ;

grant1 <= '0' ;

WHEN s2 =>

grant0 <= '0' ;

grant1 <= '1' ;

WHEN s3 =>

grant0 <= '0' ;

grant1 <= '0' ;

END CASE ;

END PROCESS output ;

END behavioral ;